# CDF Run IIB Silicon Upgrade

Temple Review
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For the CDF Collaboration

# Run 2b Silicon - Outline

Goals and Constraints

Layout

Stave Concept

Component Details

L0 design

Performance

Conclusions

# Run IIB

Run IIa luminosity goal is 2 $fb^{-1}$ delivered.
Run IIb luminosity goal is 15 $fb^{-1}$ with minimal (~6m) shutdown between them.

Run IIB working group found that L00 and SVXII will survive to ~ 4 $fb^{-1}$:

| CDF | $R_{min}$ (cm) | L ($fb^{-1}$) |
|---|---|---|
| L00 | 1.35 | 7.4 |
| L0 | 2.54 | 4.3 |
| L1 | 4.12 | 8.5 |
| L2 | 6.52 | 10.7 |
| ISL | 20 - 28 | >40 |
| DOIMs | 14 | 5.7 |

- RunIIb Working Group report used Run1a and Run1b data to estimate lifetime of Run2a detector.
- Run IIa is instrumented with 144 TLDs on SVXII outer shell and Plug face
- Preliminary results confirm WG assumptions on radial dependence of dose
- Studies and analysis of TLD data will continue

# Radiation Dose Measured Run IIA

May – Oct running

Collision dominated, but losses still present

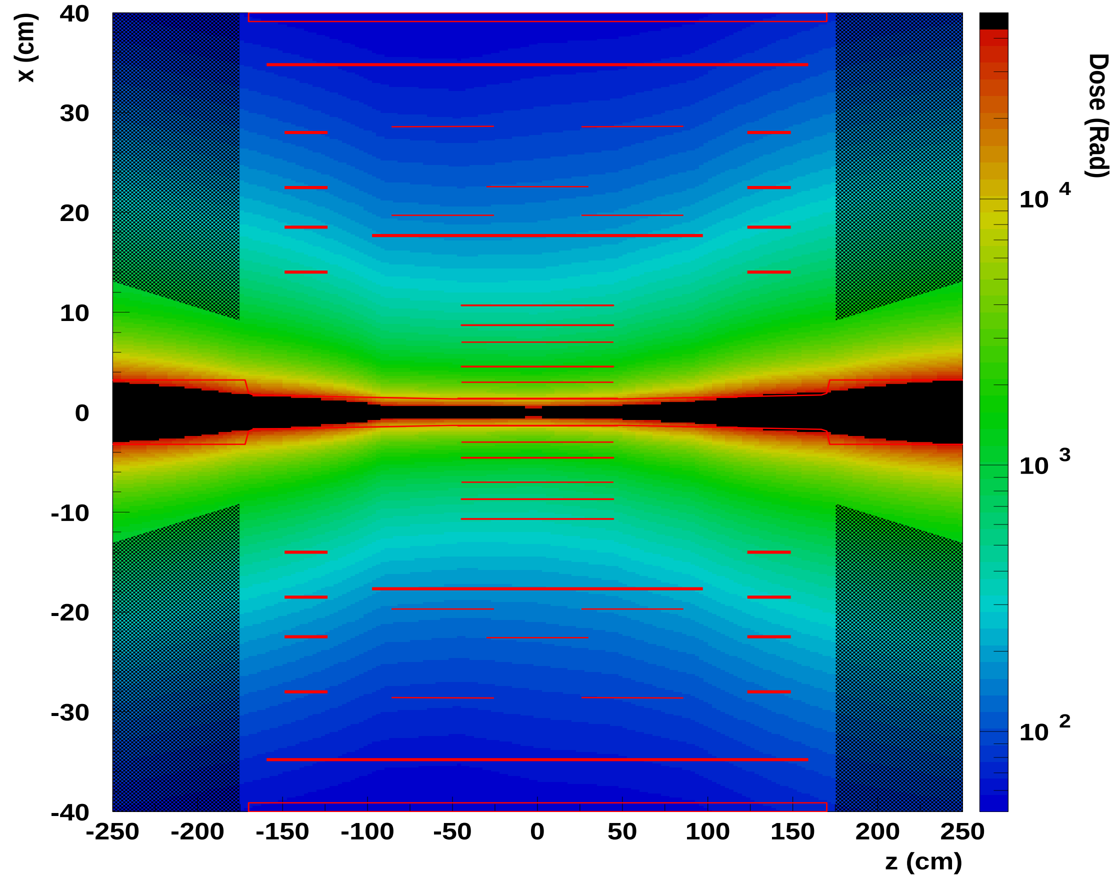
Measurements found radial and z dependence of dose

Radial dependence fit to $1/R^{\alpha}$ scaling

$\alpha$= 1.6-1.7

Run IIA lifetime estimates assumed 1.5 ± 30%

Still Valid!



# Radiation Tolerance Implications

- SVXII double sided silicon limited in bias voltage
    - Need single sided, high voltage silicon detectors (L00 style)
    - To retain tracking capability we need at least twice as many detectors: ⇒ **More silicon**
    - To survive higher radiation dose we need to operate the silicon at a lower temperature
        - **Sensors must be actively cooled**
- The current SVX3 chip (Honeywell 0.8um) cannot survive
    - New Chip: SVX4  Uses naturally rad-hard 0.25um standard technology

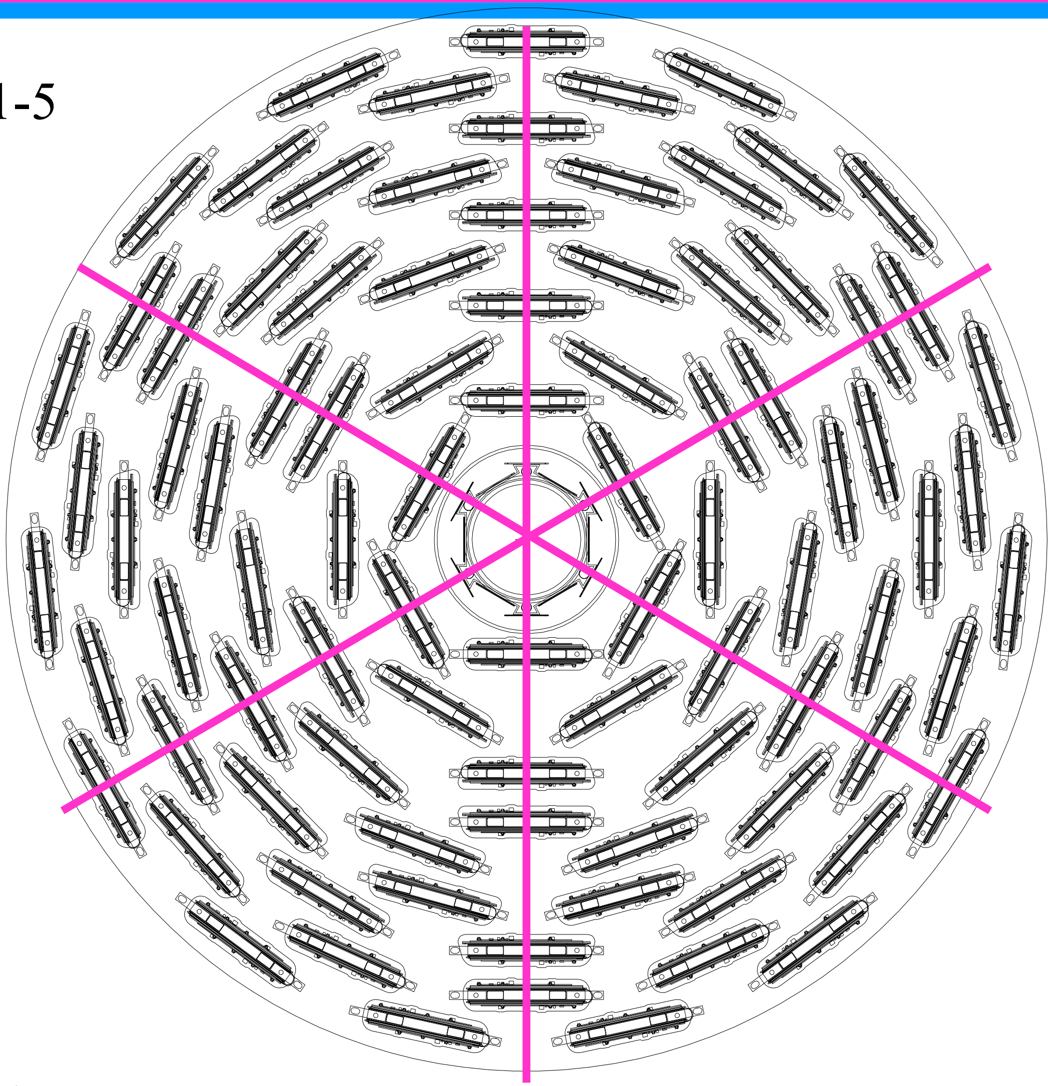
# Silicon Upgrade for Run IIB

- **Goal: Ready for installation by early 2005!**
- **Short turn around (~6m) between Run IIA and IIB**
  - Only viable option is complete replacement
- **Design Goals:**
  - Robust, simple and reliable design
  - Minimize the cost
  - Match or exceed performance of Run IIA silicon detector
  - Minimize changes to infrastructure: DAQ or cooling systems
- Pursue common solutions with D0 through task force meetings: chip, sensor specs, beampipe,…

# Run IIb layout – 6 fold symmetry

One stave design used for layers 1-5

- 1 hybrid (4chip)
- 2 sensor types (axial and SAS)
- 1 stave core structure



**Layer 0: 12 fold Axial**
**Layer 1: 6 fold Axial-Axial**
**Layer 2: 12 fold Axial-Stereo (1.2$^o$)**
**Layer 3: 18 fold Axial-Stereo (1.2$^o$)**
**Layer 4: 24 fold Axial-Stereo (1.2$^o$)**
**Layer 5: 30 fold Axial–Axial**

# Run IIB Layout Details

| Layer | Fold | Type | Radius (mm.) | pitch/RO (um) | angle | Sensors | Hybrids | #chips |
|---|---|---|---|---|---|---|---|---|
| 0 | 12 | Axial | 21.0 and 25.0 | 50/25 | 0 | 144 | 72 | 144 |
| 1 | 6 | Axial | 35.5 and 43.5 | 75/37.5 | 0 | 72 | 36 | 144 |
| 1 | 6 | Axial | 40.0 and 48.0 | 75/37.5 | 0 | 72 | 36 | 144 |
| 2 | 12 | Axial | 59.5 and 74.75 | 75/37.5 | 0 | 144 | 72 | 288 |
| 2 | 12 | Stereo | 64.0 and 79.25 | 80/40 | 2.5 | 144 | 72 | 288 |
| 3 | 18 | Stereo | 90.75 and 104.5 | 80/40 | 2.5 | 216 | 108 | 432 |
| 3 | 18 | Axial | 95.25 and 109.0 | 75/37.5 | 0 | 216 | 108 | 432 |
| 4 | 24 | Stereo | 119.25 and 133.0 | 80/40 | 2.5 | 288 | 144 | 576 |
| 4 | 24 | Axial | 123.75 and 137.5 | 75/37.5 | 0 | 288 | 144 | 576 |
| 5 | 30 | Axial | 147.5 and 161.5 | 75/37.5 | 0 | 360 | 180 | 720 |
| 5 | 30 | Axial | 152.0 and 166.0 | 75/37.5 | 0 | 360 | 180 | 720 |
| | | | | Totals | | 2304 | 1152 | 4464 |
| | | | | Totals SVXII + L00 | | 864 | 768 | 3276 |
| | | | | Total Increase | | 267% | 150% | 136% |
| | | | | % outer layers | | 94% | 94% | 97% |

94% of sensors and hybrids are 4-chip

# Number of Axial hits in L0-5 vs phi

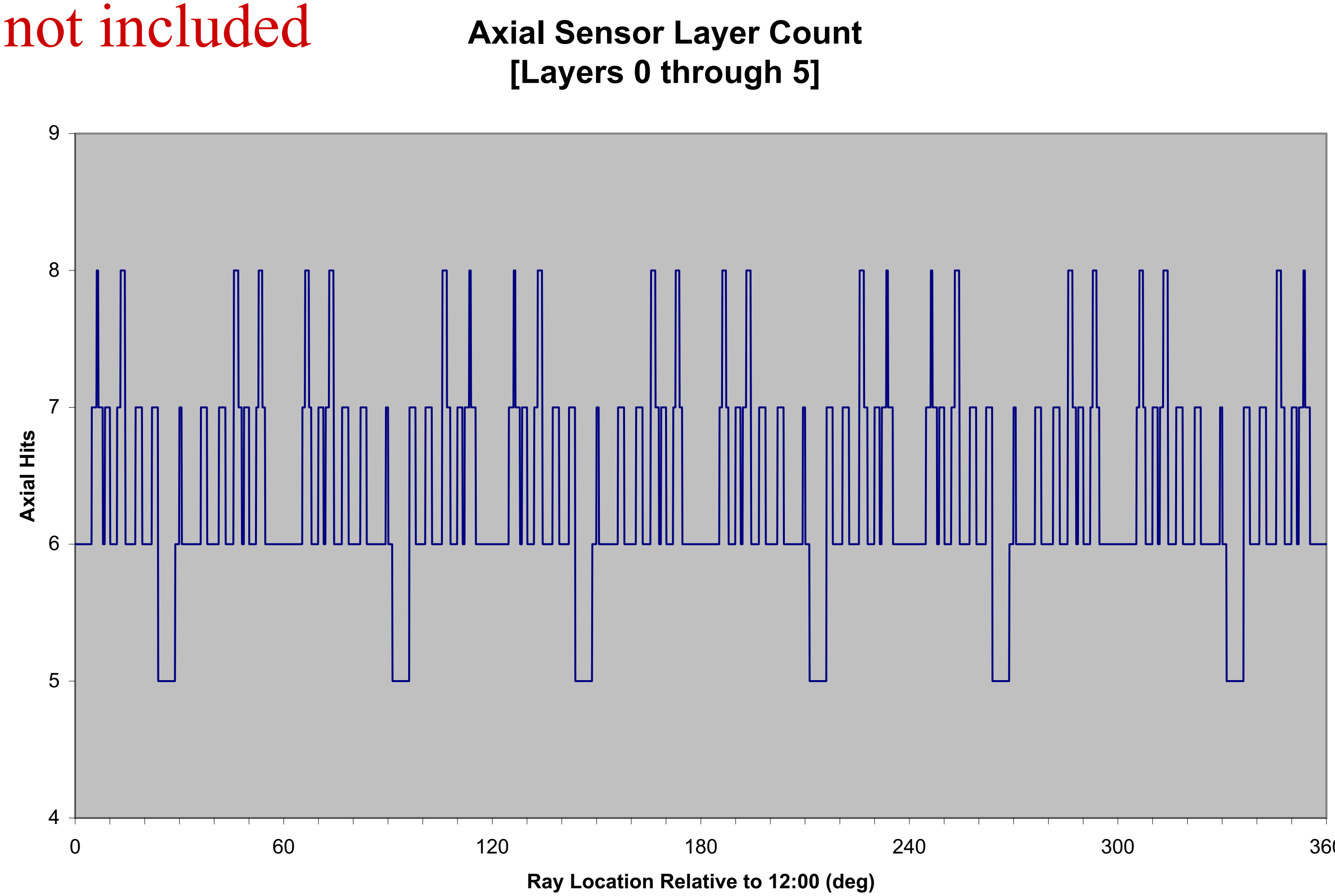
Double axial hits not included

8 hits – 7%

7-hits – 29%

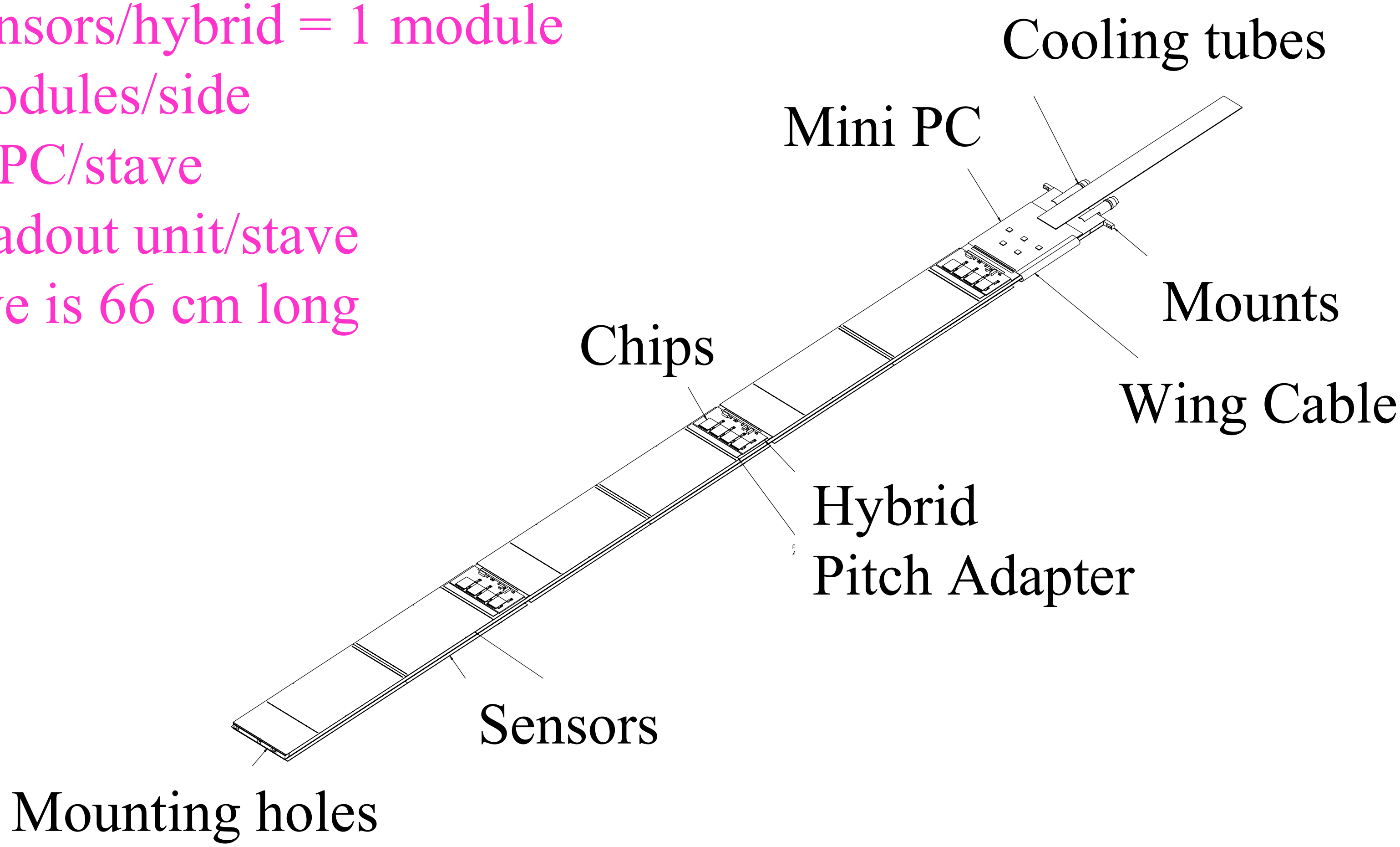
6-hits – 56%

5-hits – 8%

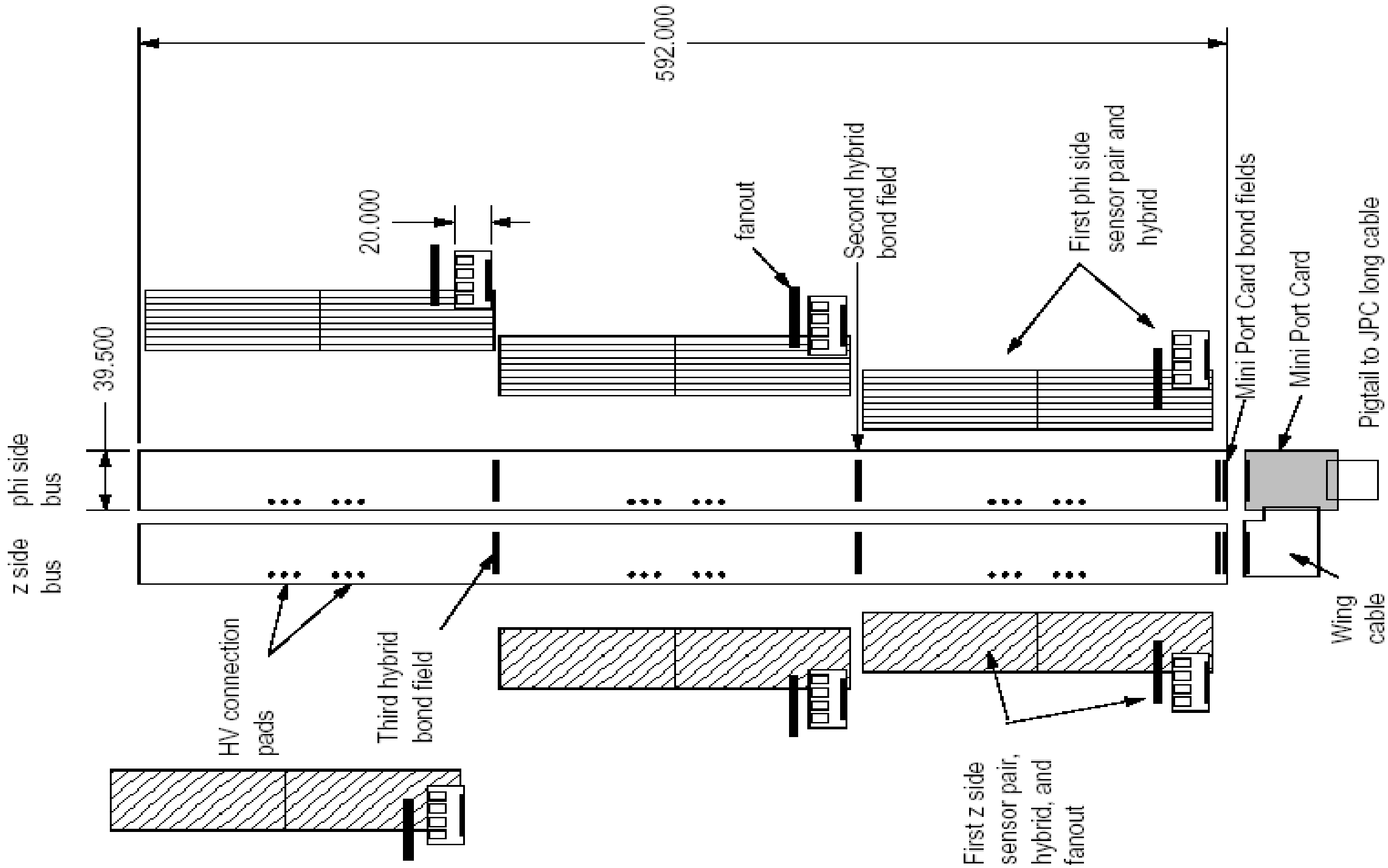


# Run IIB Stave

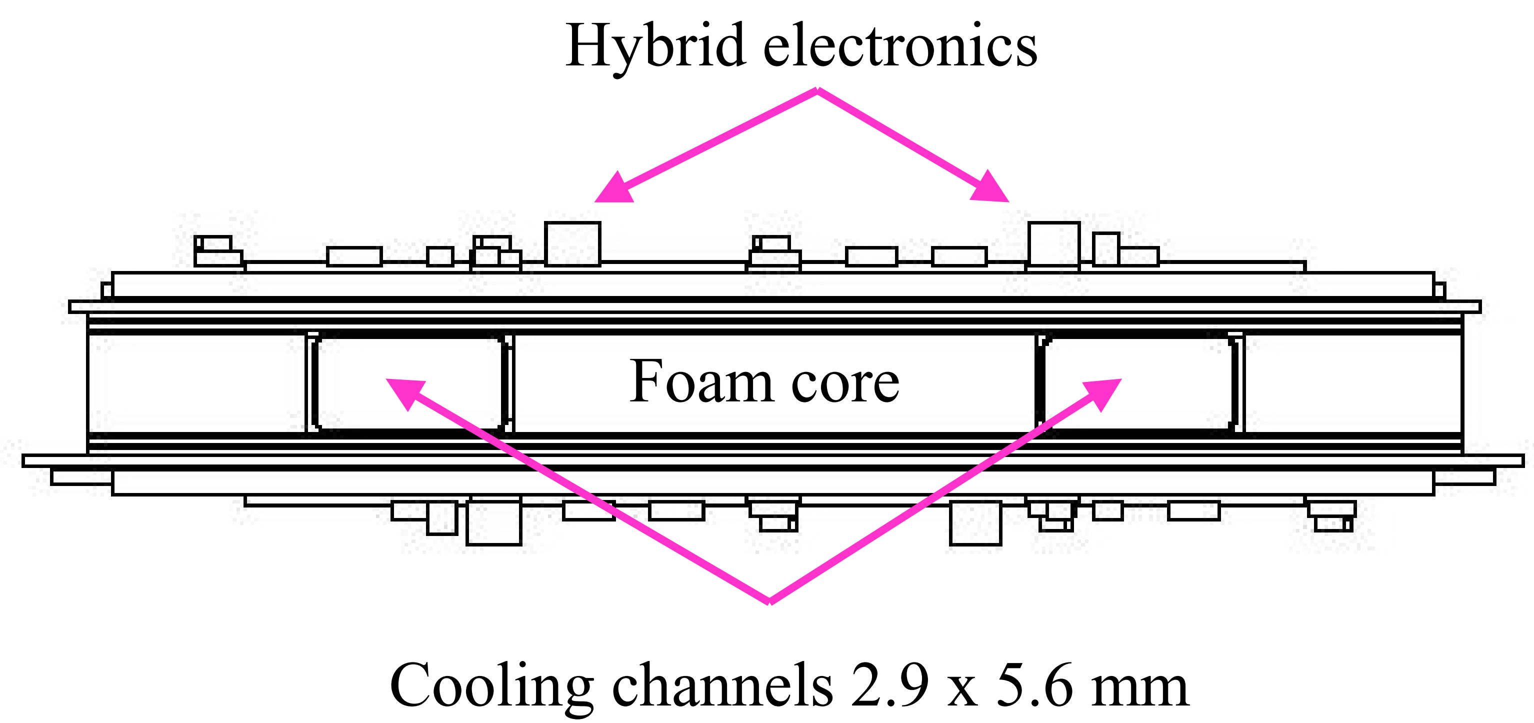
- 2 sensors/hybrid = 1 module
- 3 modules/side
- 1 MPC/stave
- 1 readout unit/stave
- Stave is 66 cm long



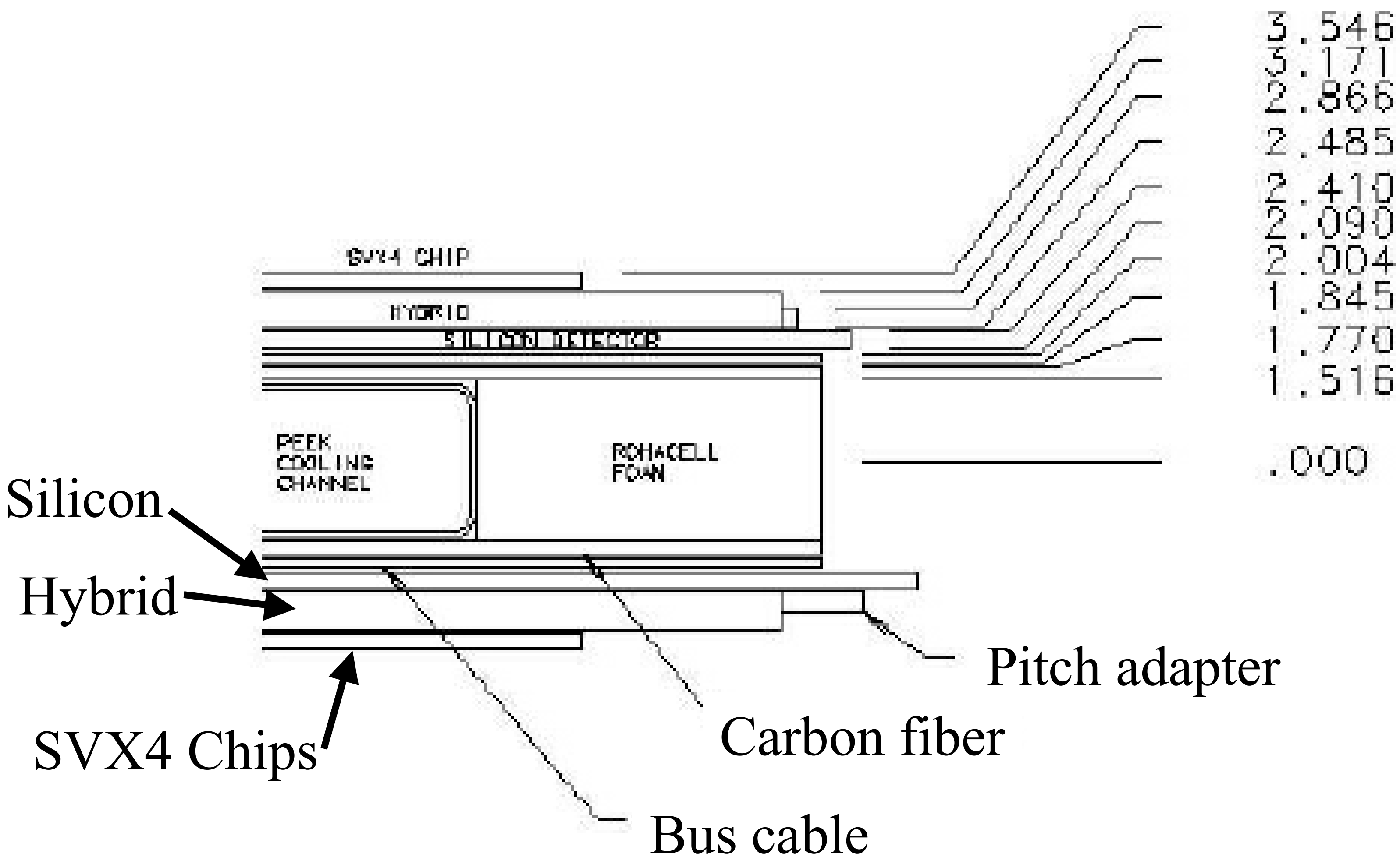
# Stave Components



# Stave End View



# Stave details

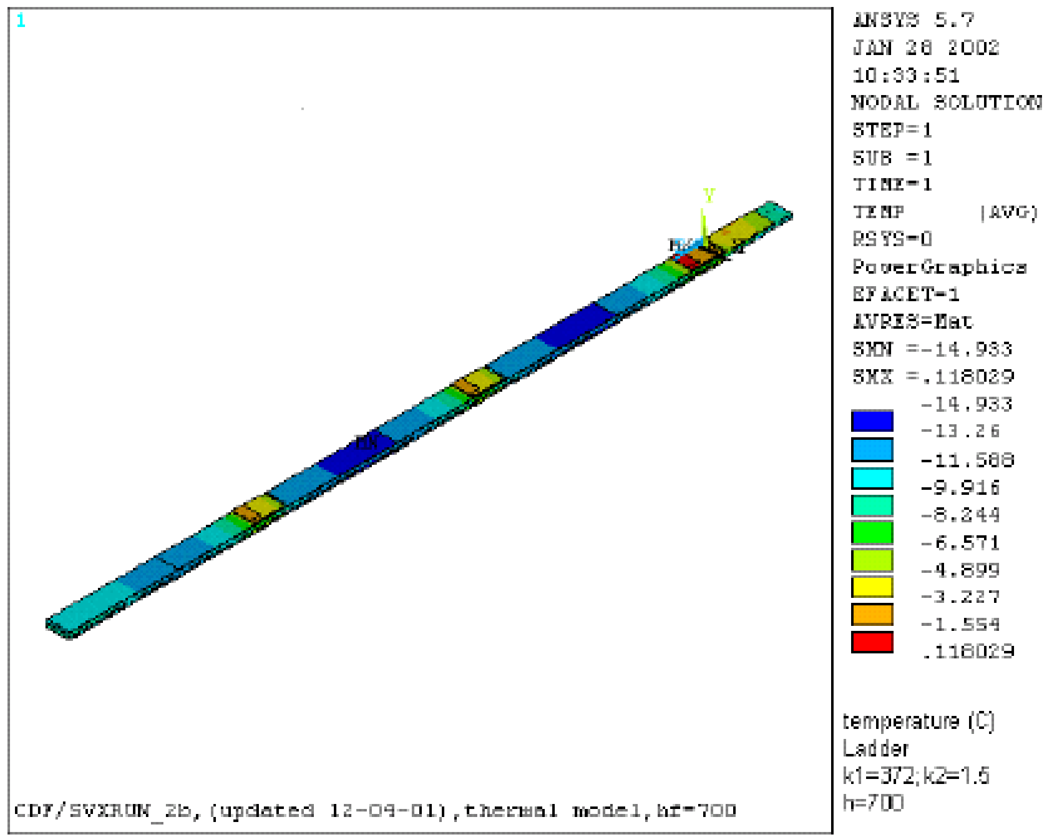


# Radiation Damage and Cooling

- Keep silicon cool to limit the amount of noise increase due to leakage current and limit the reverse annealing effect
- Studies of these effects set temperature limits: for S/N >10 for 30 $fb^{-1}$
  - Layers 4-5: T<15$^{o}$ C
  - Layers 2 and 3: T<10$^{o}$ C
  - Layers 0 and 1: T<-5$^{o}$ C
- Requires active cooling of staves
  - Cooling tubes integrated into stave structure
- Total heat load very similar to Run IIA ~3KW
- Plan to use existing cooling system with increased glycol concentration (43%) for operation at -15$^{o}$C

# Cooling Studies

- Heat from chips is spread through BeO hybrid
- Then transferred through multiple adhesive layers, Silicon, bus cable, and CF
- Cooling tube is PEEK 0.1mm thick and 5.6 mm flat area
- Coolant T=-15C
- Convection to +10C gas
- Silicon temp < 0C everywhere
- Important quantity is average over a strip:
  - **Axial: –10C**
  - **Shortest Stereo strip: –4C**



# Stave Material- part 1

| | | Mass (g) | %RL | Percent of Total %RL |
|---|---|---|---|---|
| **Sensors** | | **39.3** | **0.72** | **39.3** |
| | Axial | 16.348 | 0.32 | 17.2 |
| | Stereo | 18.586 | 0.36 | 19.5 |
| | Epoxy | 4.283 | 0.05 | 2.5 |
| | Silver | 0.049 | 0.00 | 0.1 |
| **Hybrids** | | **11.7** | **0.24** | **13.0** |
| | BeO | 4.938 | 0.05 | 2.7 |
| | Glass | 1.154 | 0.02 | 1.0 |
| | Gold | 0.792 | 0.05 | 2.8 |
| | Capacitors | 1.065 | 0.04 | 2.2 |
| | Resistors | 0.058 | 0.00 | 0.0 |
| | Solder | 0.451 | 0.02 | 1.3 |
| | Silver | 0.068 | 0.00 | 0.2 |
| | SVX4 Die | 0.999 | 0.02 | 1.0 |
| | Pitch Adapter | 1.483 | 0.02 | 1.2 |
| | Epoxy | 0.609 | 0.01 | 0.3 |
| | Wirebonds | 0.049 | 0.00 | 0.1 |

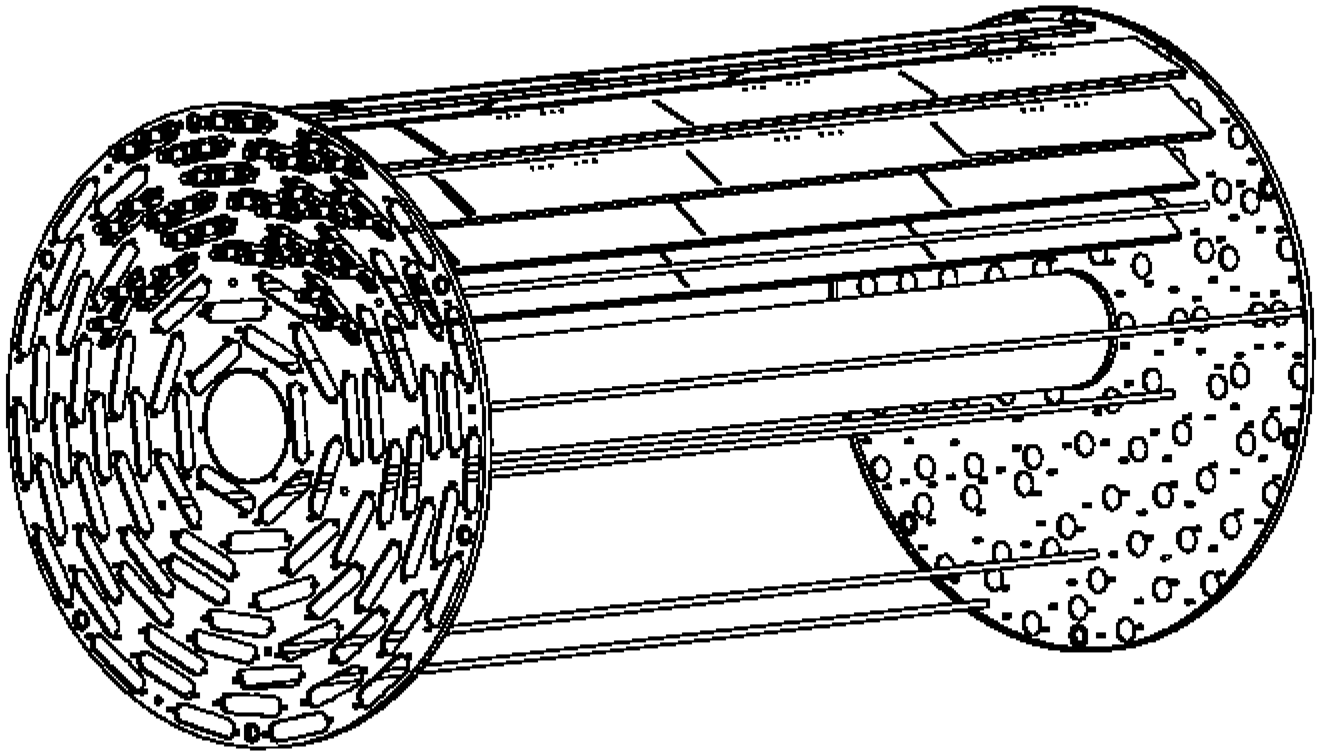
Total/Stave:
1.84% RL
124 g

# Stave Material – part 2

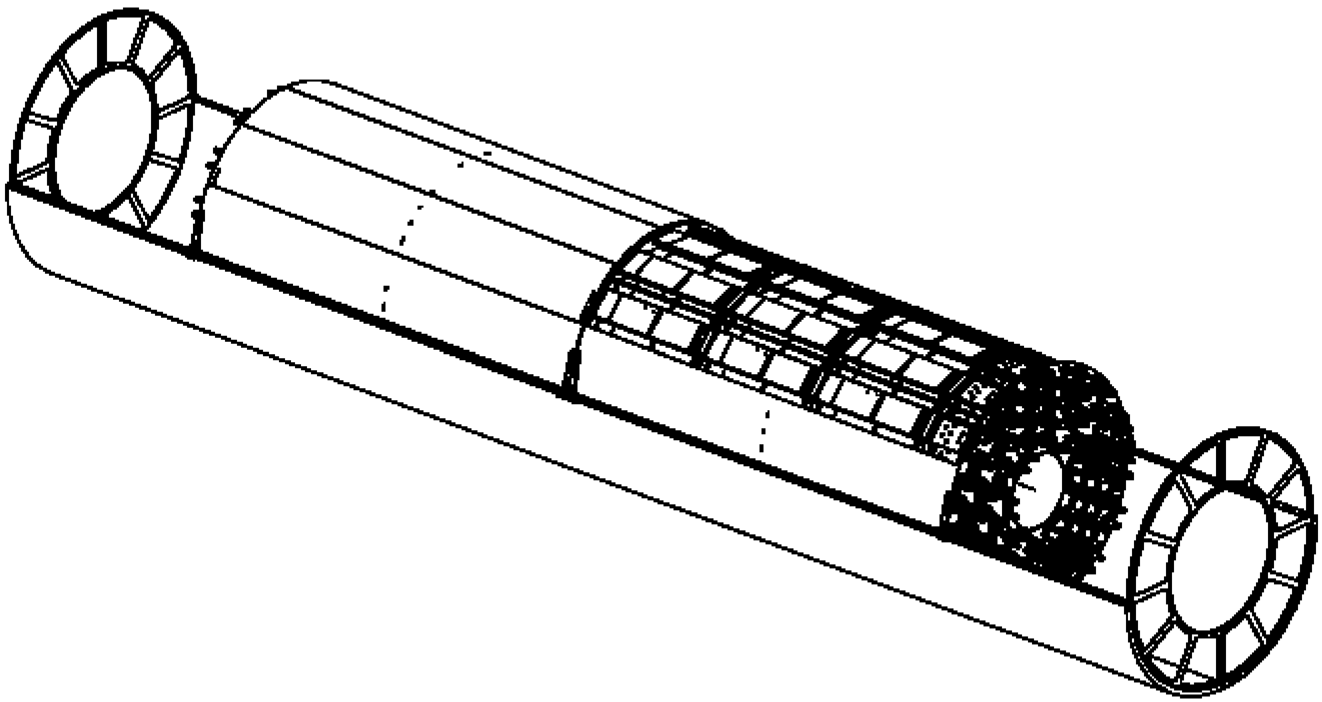
| | | Mass (g) | %RL | Percent of Total %RL |
|---|---|---|---|---|
| **Bus Cable** | | **19.6** | **0.32** | **17.4** |
| | Kapton | 4.853 | 0.05 | 2.9 |
| | Copper | 4.467 | 0.15 | 8.0 |
| | Aluminum | 1.622 | 0.03 | 1.5 |
| | Interlayer Glue | 4.333 | 0.05 | 2.5 |
| | Epoxy | 4.333 | 0.05 | 2.5 |
| **Ladder Core** | | **51.3** | **0.54** | **29.3** |
| | Skin Carbon | 14.904 | 0.15 | 8.0 |
| | Skin Epoxy | 5.777 | 0.06 | 3.3 |
| | PEEK Tubing | 2.306 | 0.02 | 1.3 |
| | Coolant | 16.597 | 0.19 | 10.2 |
| | Foam | 2.464 | 0.03 | 1.4 |
| | Epoxy | 8.665 | 0.09 | 5.0 |
| | Inner Mount | 0.568 | 0.00 | 0.2 |
| **Support Hardware** | | **1.9** | **0.02** | **1.1** |
| Z = 0 End Support | | | | |
| | Inner Bulkhead Carbon | 1.342 | 0.01 | 0.7 |
| | Inner Bulkhead Epoxy | 0.520 | 0.01 | 0.3 |
| | Pins | 0.072 | 0.00 | 0.1 |

Total/Stave:
1.84% RL
124 g

# Barrel assembly

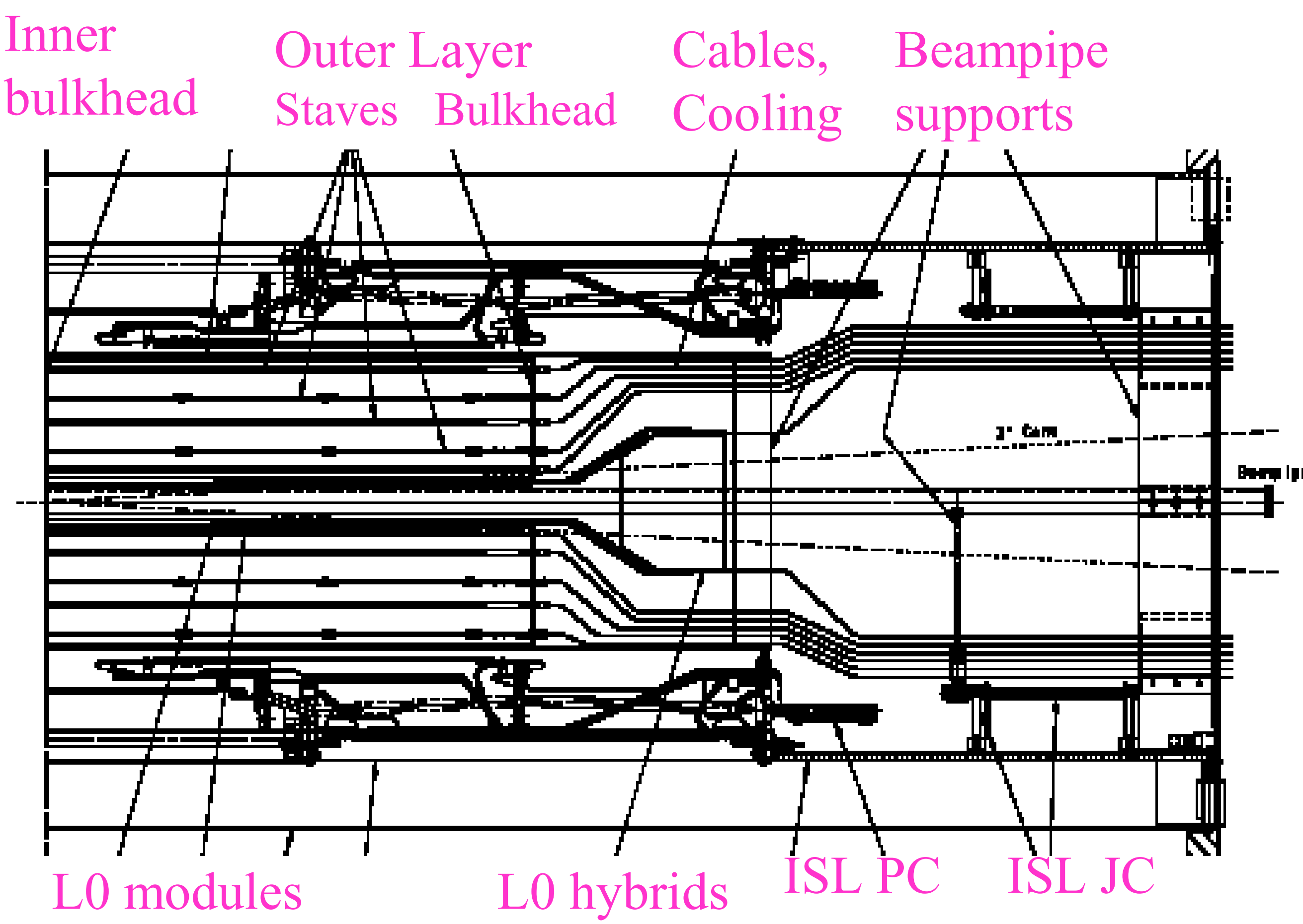


# Barrel in Spacetube



# Side View of Run IIB

- L0 sensors
  - 74.7mm long
  - 93cm total
- L1-5 sensors
  - 96 mm long
  - 117 cm total



# Run IIB Layout Summary

- Uniform stave (ladder) design for ~94% of the detector

  L1-5 = 180 staves - only one set of fixturing to develop

  (SVXIIA had 180 ladders, 5 different sizes, 36 of each size)

  L0 ~ L00 type construction

- Small number of different style parts

  Only 2 types of hybrids – 4 chip on outer layers, 2 chip on Layer 0

  L1-5 have 2 sensor types (axial and small angle)

  L0 has 1 type of sensors (L00 in Run IIa had 2 types)

- Construction flexibility

  Stave design independent of sensor type (axial-SA, or AA)

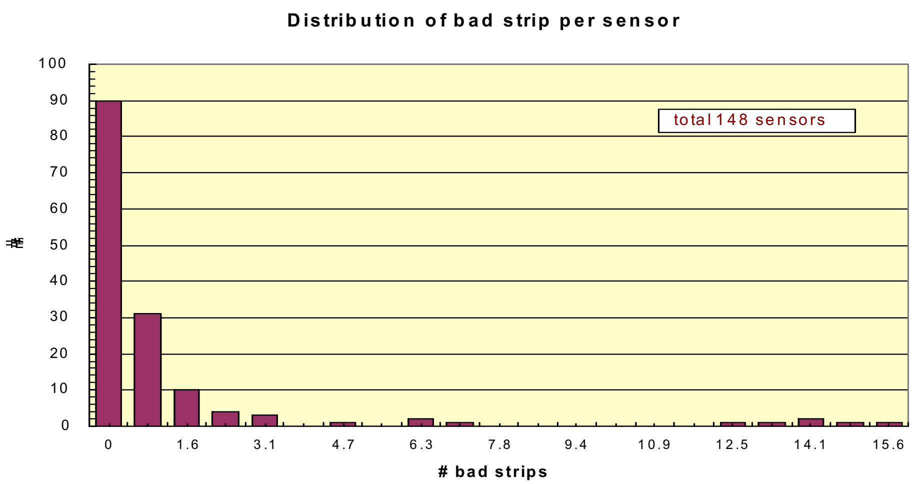
  Can swap Layers 2-5 → descoping possible late in project

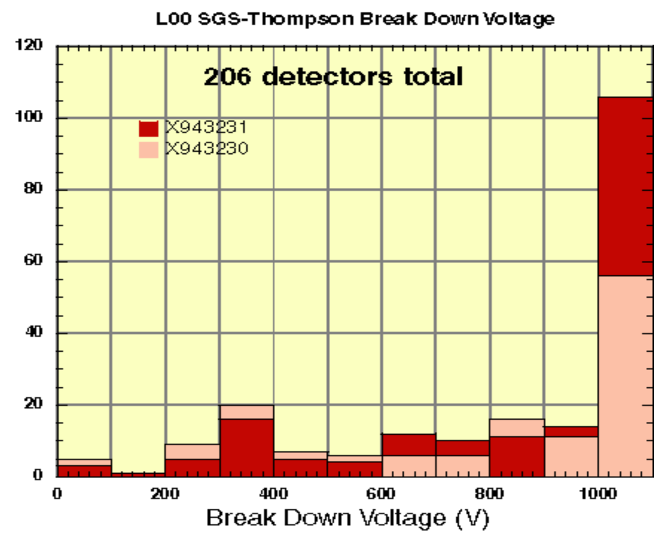
# Run IIB Status –outer layers

- Spring 2002
  - Concentrate on prototyping of outer layer components for modules and staves
  - Prototype sensors have been ordered, expected in July
  - Module fixture for sensor to sensor gluing has been fabricated and tested
  - SVX4 prototype chip design is finished and submitted for fabrication
  - Hybrid and bus cable designs finalized and ordered
  - Miniportcard design finished and submitted
  - All components should be in hand by July 02

# Silicon Sensors

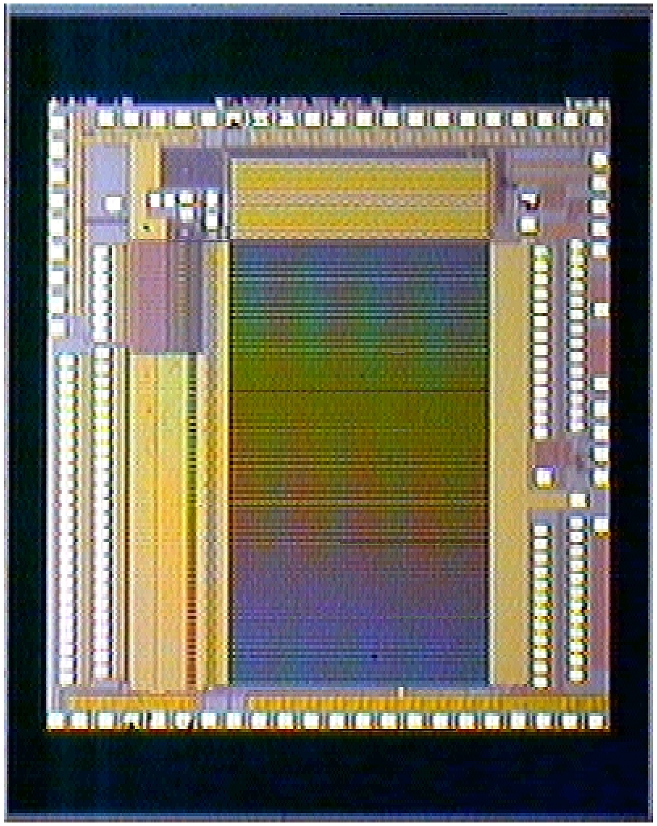
- All detectors are single sided and based on the high voltage operation layout (CMS,ATLAS,L00)
  - Easy to build, test and handle
  - Minimal R&D necessary
  - High yield and a minimum number of problematic channels is expected (<1% in most of the detectors)
  - Mask Designs nearing completion – prototype orders in progress
- Experience with L00 Sensors:



# SVX4 Chip

- The chip design was finished and submitted for manufacturing April 1! This is the single most critical item for the schedule.
- Expect chips back at end of May.
- Chips ready for hybrids by mid July
- This chip has undergone more simulation than any previous SVX chip.
  - ~Dec. – March spent simulating
  - Test chips came back in early August – entire frontend (preamp + pipeline) functioned!
  - Chips irradiated to 16 Mrad with Co-60 facility, no changes observed
  - S/N 30% better than SVX3
  - CDF and D0 use same chip



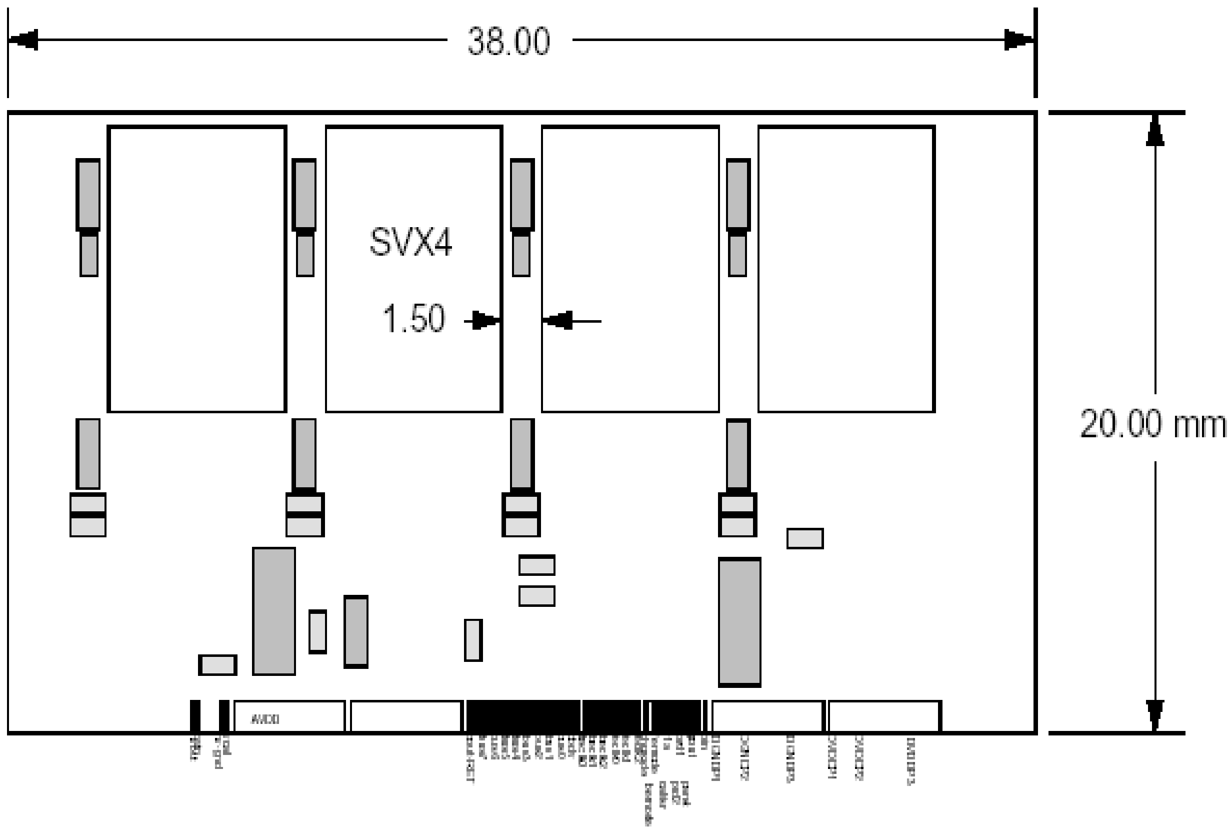
# Outer Layer Hybrid Layout

Same technology used on L00 with larger pitch and traces

100µm trace/100µm space and 125 µm vias with 200 um spacing

Can fit a power bus and signal traces on a single layer, keeping the total number of layers to 4

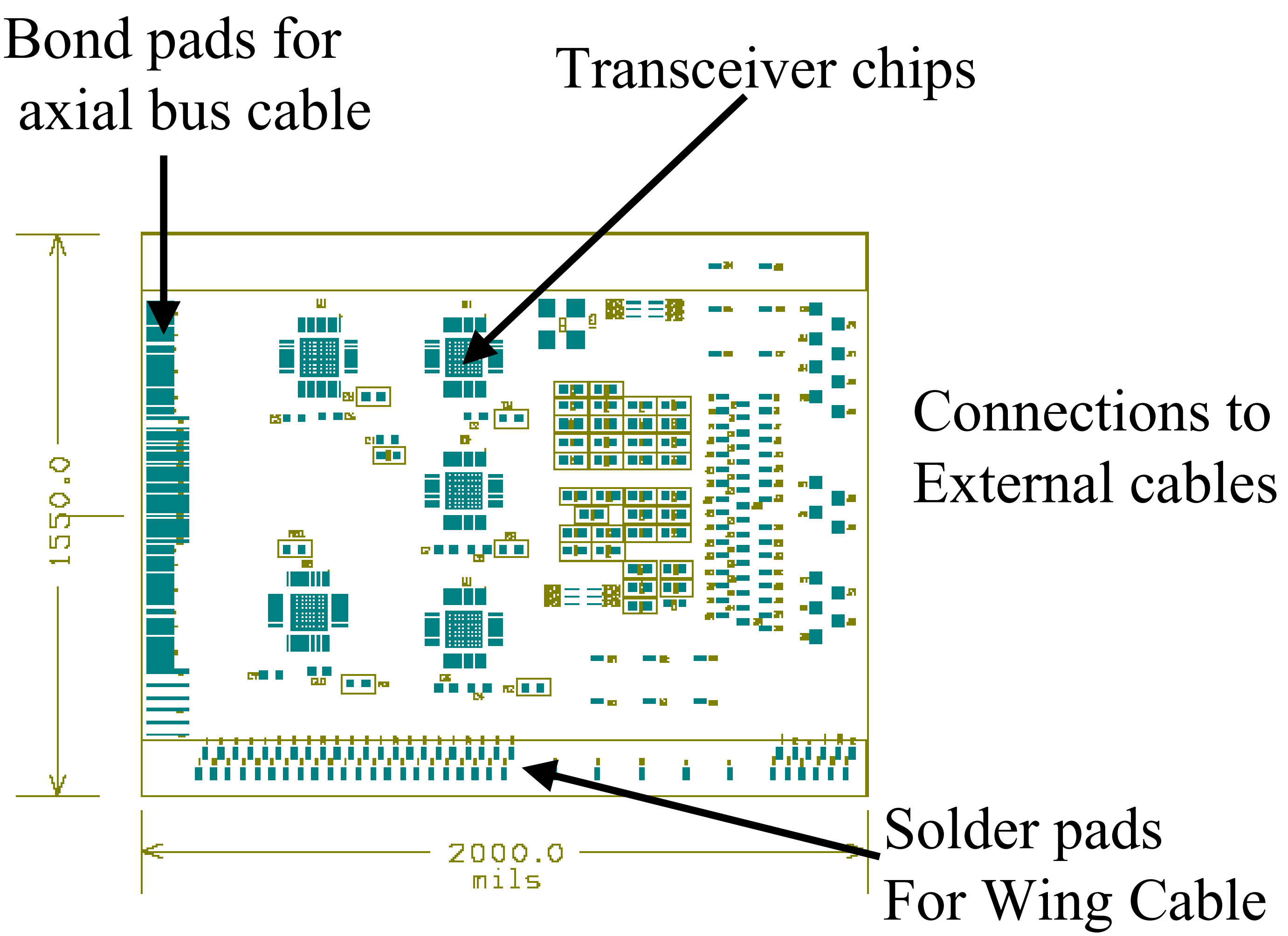
Result is a much smaller hybrid wrt SVXII



# Mini Portcard Layout

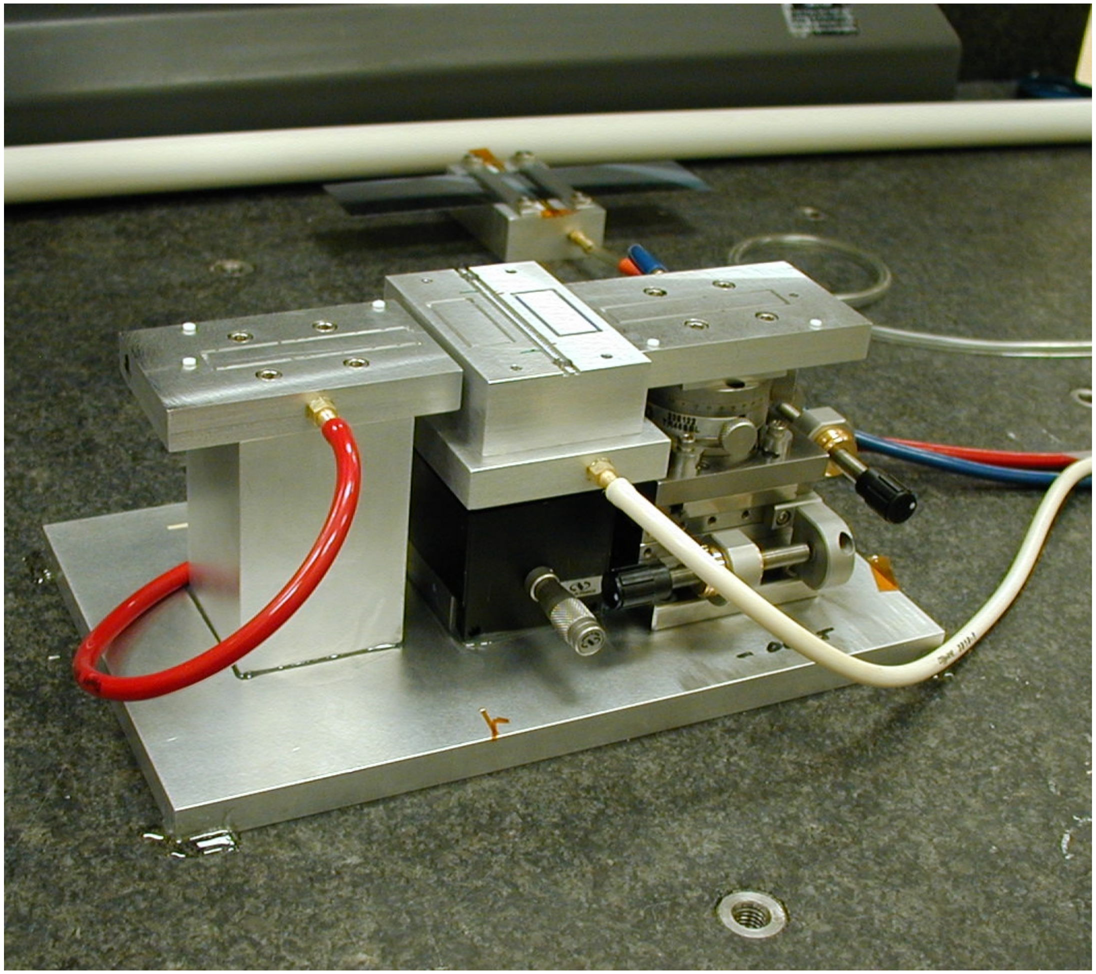
Use BeO for substrate (380um thick)

3 layers of traces
Plus power and ground

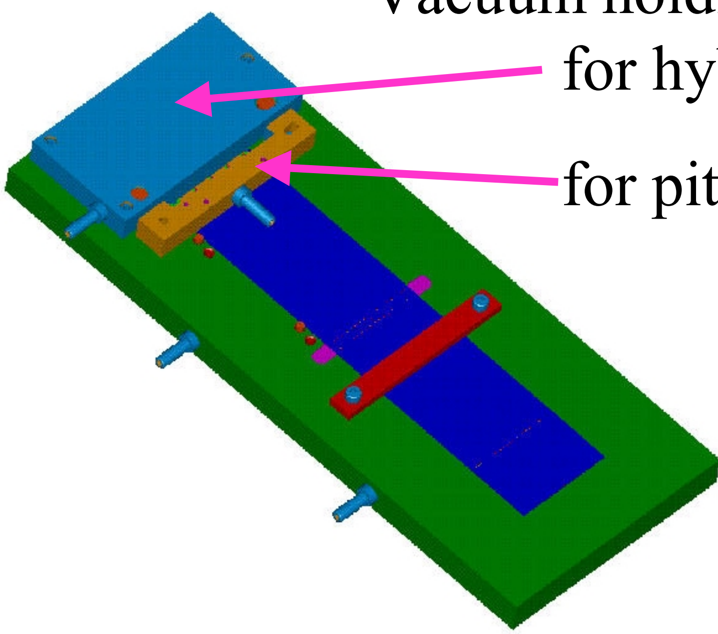


# Sensor to sensor gluing fixture

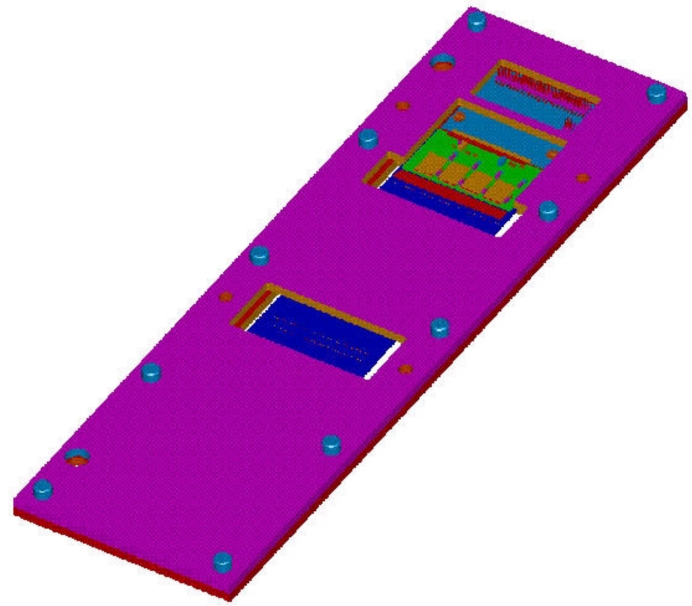
- Similar to L00 style fixtures
- Sensors under vacuum
- Glue applied to area on center block
- Center block is raised to meet sensors
- Block + sensors can be removed for curing
- Frees up fixture for a new module
- Tests found that sensor position is very stable
- Assembly process is faster than expected



# Other outer layer module fixtures




Hybrid and pitch adapter gluing fixture



Module storage frame

# Layer 0 Design

- Inner Layer (L0) follows Run IIa L00 design
  - Smallest possible pitch – 25/50 micron pitch
  - Fine pitch cables connect sensors to hybrids
  - Hybrids are located out of tracking volume (~z=70cm)
  - Smallest possible R
    - ID set to slide over Beampipe end flange (RunIIa)
  - Hybrids ~similar to outer layer, but 2 chips
  - Will be supported by outer barrel (not beampipe)
- Limit cost and risk in assembly process
  - Fine Pitch Signal Cables (L00 style) used only on L0
  - Having hybrids glued to silicon for majority of layers is great benefit in terms of ease of assembly, handling, testing, commissioning
  - Low mass construction is of utmost importance for 1st measurement
  - Additional material/layer with stave design is small (0.3%X0) and effect is reduced for outer layers.
- Prototype efforts on cables are underway using L00 layout

# L0 Layout

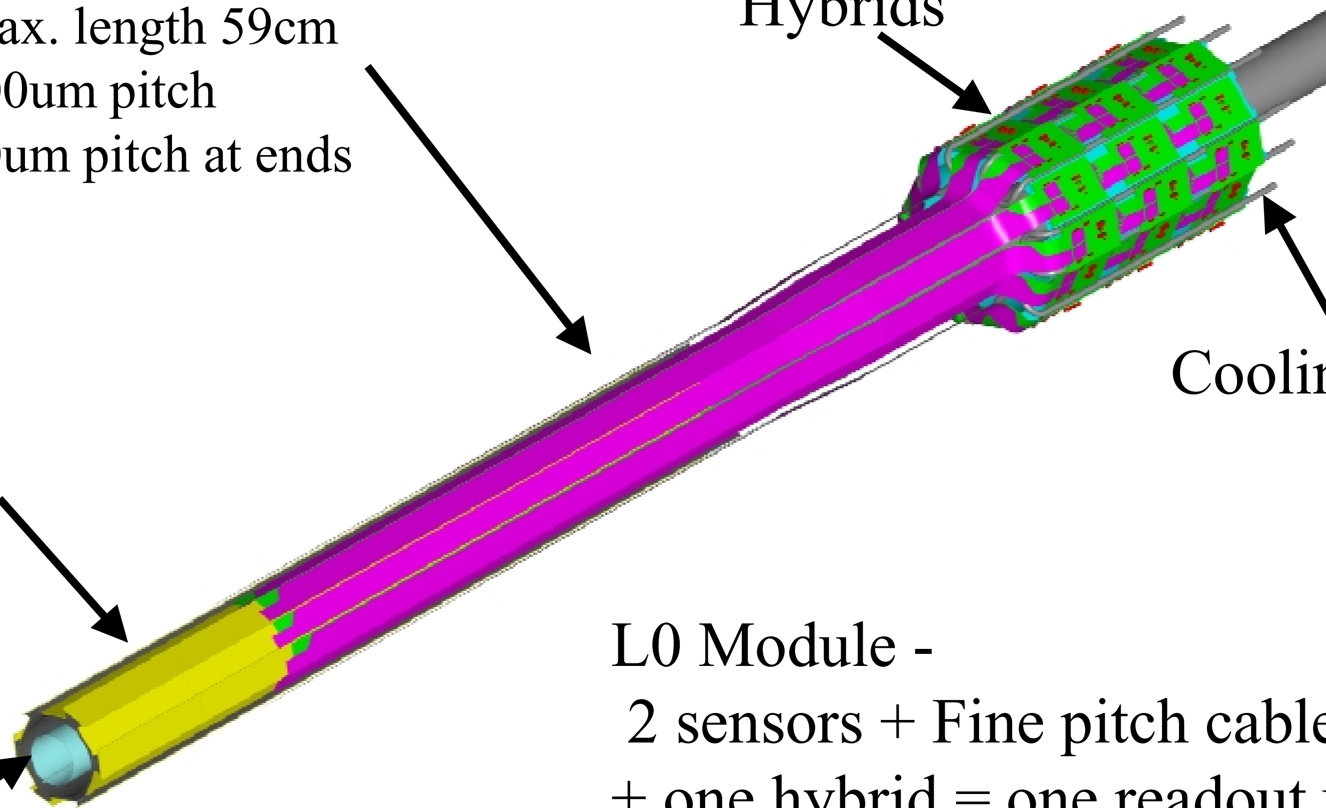
Fine pitch cables

Max. length 59cm

100um pitch

50um pitch at ends

Hybrids



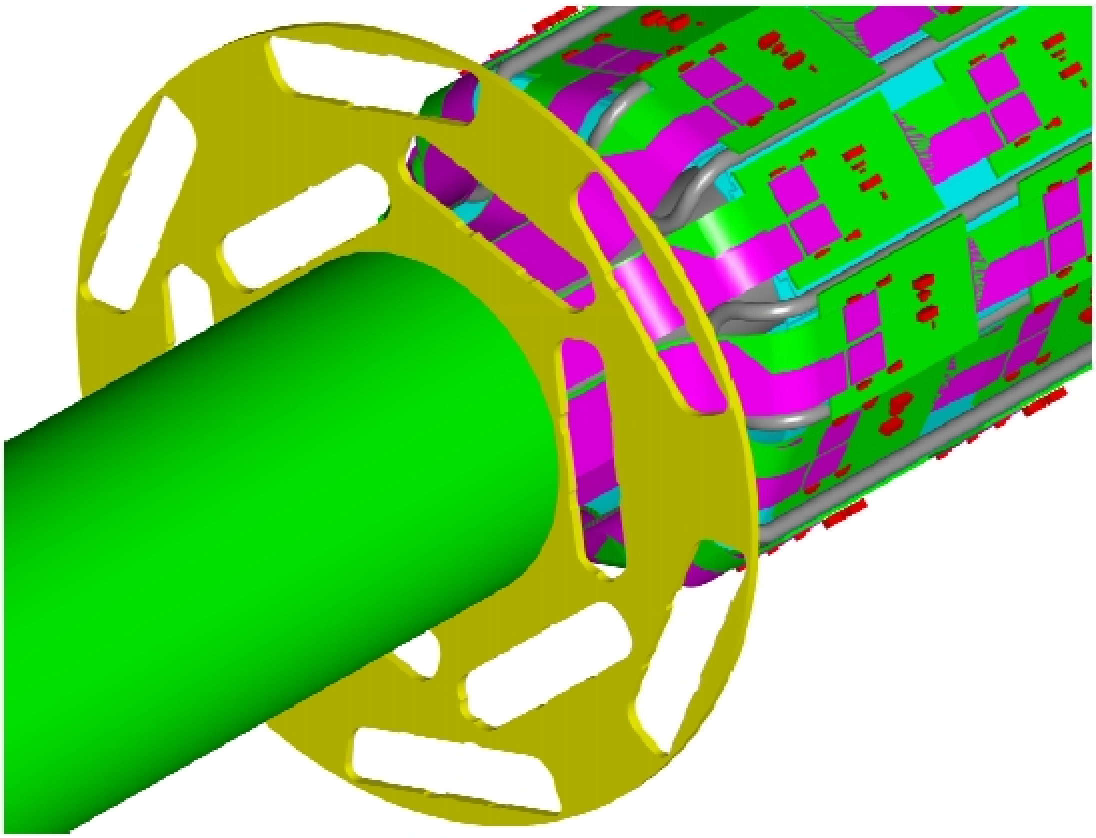
Cooling tubes

Sensors

L0 Module -
2 sensors + Fine pitch cables
+ one hybrid = one readout unit

Beampipe and CF support

# L0 hybrids and cables



Cable flare out in radius (to ~4cm) after passing through bulkhead

Cables from successive modules pass underneath hybrids from lower z modules

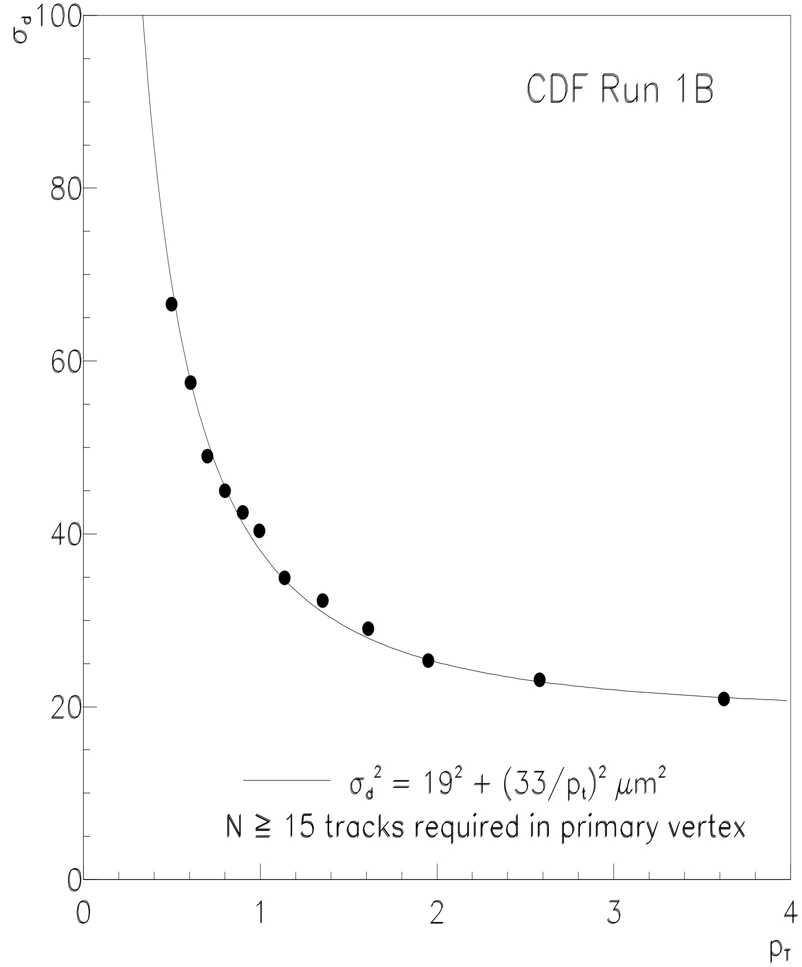
Cooling tubes integrated into hybrid support structure

# DAQ Changes from Run IIA

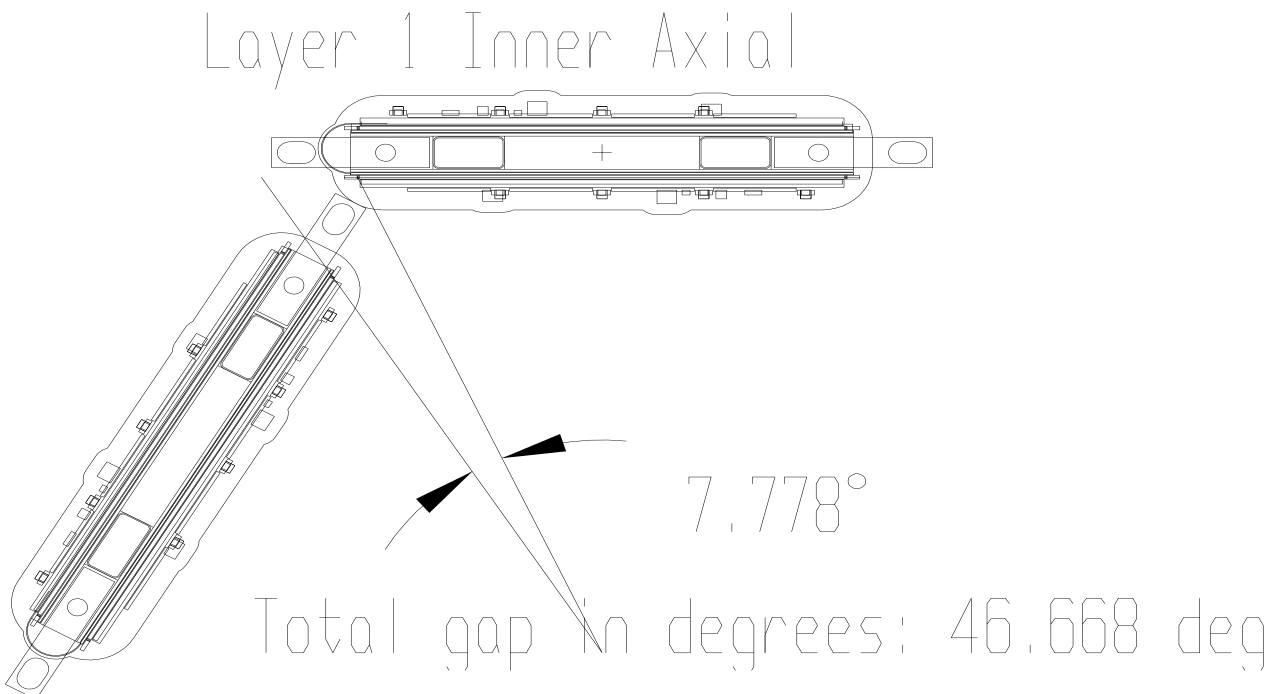
- New chip requires changes in front end of DAQ: 2.5V instead of 5V
- New hybrids (smaller!)
- Optical components unavailable and not rad hard:
  - New mini portcards (smaller, minimal active components)
  - New Fiber Transition Modules (No Fibers!, use copper instead)
  - Copper cables are outside tracking region - off end of staves
  - Test stand with Copper readout setup and tested!
- New Power Supplies: off-the-shelf, not custom
- No changes upstream of the FTMs
- Reduced mass in tracking volume and improved accessibility
- Significant reduction in number of different components
- Number of readout chains fits in existing infrastructure
- SVT can be enhanced to work with Run IIB layout
  - Modifications similar to those already made for L00

# Performance issues - parametric

- Analytic program
  - Input hit resolutions and material
  - Calculate IP or pointing resolution as a function of track momentum
- Run 1b data comparison
  - Calculation: 13 ⊕ 34/pt [μm]
  - Then include primary vertex uncertainty (±10 μm) and wedge to wedge misalignments (± 10 μm)
    - 19 ⊕ 34/pt
  - Measurement: 19 ⊕ 33/pt
- Very good agreement! Can use to estimate performance of Run 2A and 2B Detectors



# Layer 1 has gaps




Layer 1 inner coverage is 87%

Layer 1 outer coverage is 79%

# Study effect of Layer 1 gaps

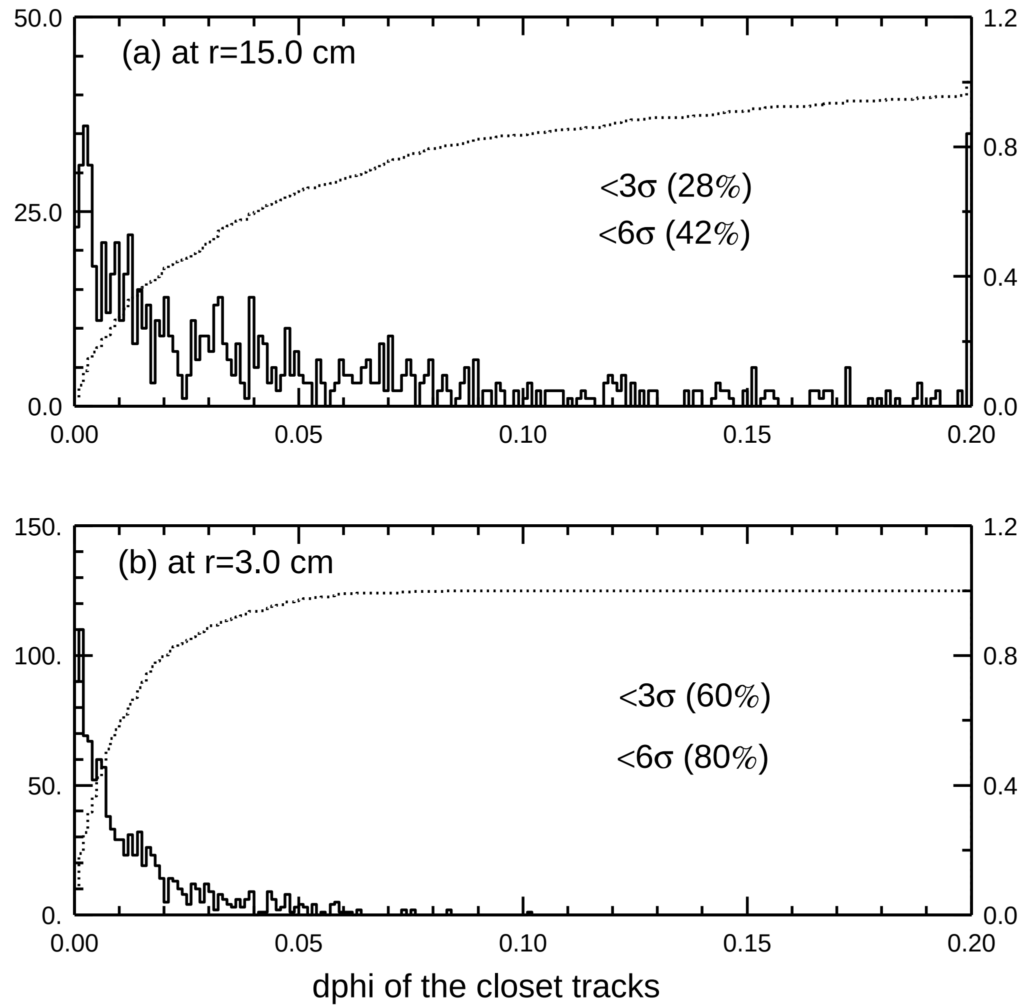
- Studied relative impact parameter resolution with analytic program
- Take into account material and produce results with Multiple Scattering
- R-phi resolutions:

| r-phi | asym. (um) | Pt= 2GeV (um) | | |
|---|---|---|---|---|
| **Configuration** | | | | |
| All layers | 6 | 25 | | |
| No Layer 1 | 7.5 | 27 | | |
| No Layer 0 | 9 | 51 | | |
| No Layer 0,1 | 15 | 79 | | |
| **L1 30 deg incident angle (60% degradation in resolution)** | | | | |
| All layers | 7.2 | 26 | | |
| No layer 0 | 13 | 58 | | |

Note, Run 1B additional uncertainties were ~10um from beam spot and ~10um from alignment.

# Potential of Double axial staves

- Generator level study,
- Use hits on opposite sides of a stave to construct a stub with a slope.
- Look at tracks pointing in from ISL/COT
- Match slope from external track to slope in stave
- Study indicates that 72% of potential confusion could be rejected.
- More studies needed



# Number of Stereo layers

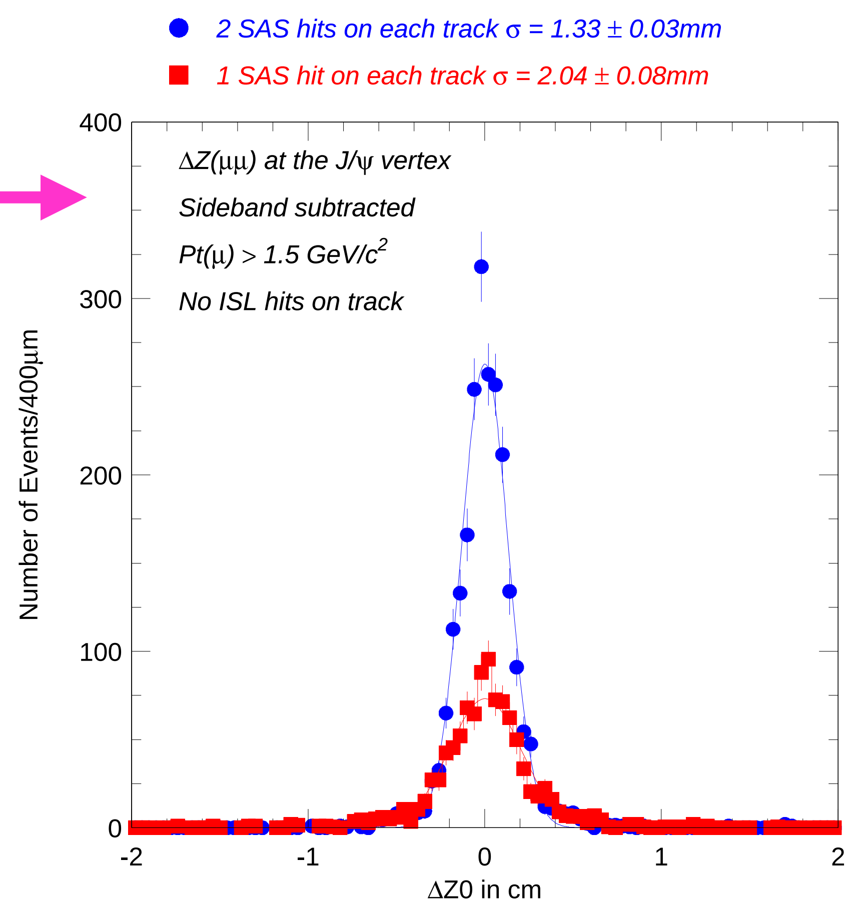
- Study with MC and with Run IIa data
- J/psi Data – No ISL stereo, Max number SAS = 2

- Run IIa MC Resolution on the z vertex (one ISL hit already required)

  2.5cm with 2 SAS layers

  1.3cm with 3 SAS layers

  1.1cm with 4 SAS layers



# Conclusions

- Highly modular, streamlined design for the Run IIB Silicon Detector
- Design relies heavily on experience with previous silicon detectors at CDF (SVX, SVX', SVXIIa, L00 and ISL)
- Maintains the tracking capability of the CDF detector
- Total mass in tracking volume is reduced
- DAQ simplified, active components are more accessible
- Design and prototyping efforts are underway for outer layer components – orders have been placed for all stave components
- Next talk – Cost and Schedule

# Tracking Studies – dropping layer 4 or 5

- Use Run 2A simulation (well studied), ISAJET MC and ttbar events.
- Study tracking (OI) and b-tagging efficiencies for different configurations

  A: Baseline = Run 2a = L00 + 5 SVX layers + ISL and COT

  B: Drop Layer 5 of SVXII (~ same effect on b-tag eff as loss of inner COT)

  C: Inner axial and stereo layers of COT dead and drop L5

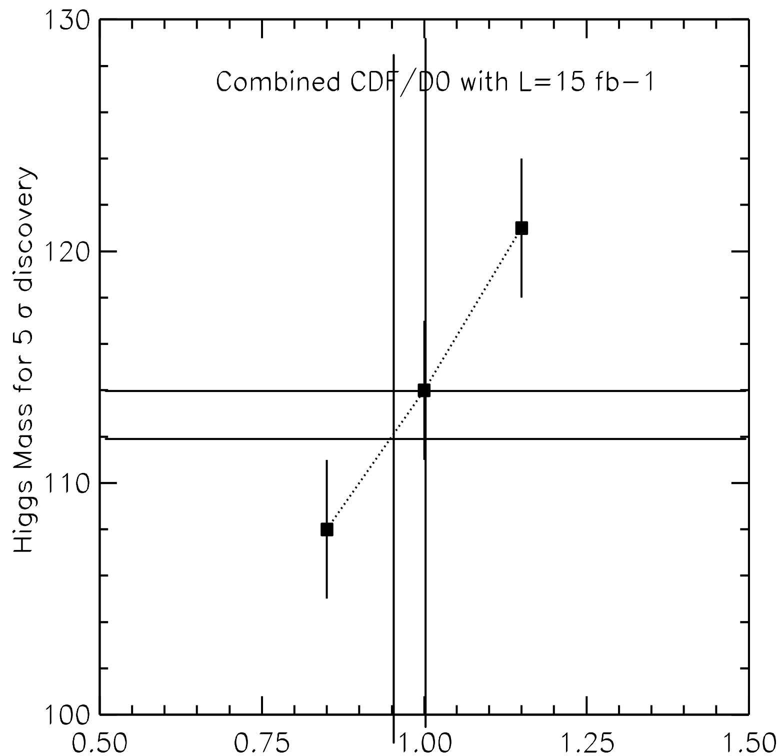
  D: Inner COT layers dead and drop L4
- b-tag ≡ 3σ Lxy for a jet. Results for 1000 events, stat. unc.~1.3%
- Fake track ≡ (MC d0 – found d0)>3σ for a prompt track. 100 Evts,stat. unc. ~0.5%

| | B-tag Eff. (%) | % Change |
|---|---|---|
| A | 58.8 | - |
| B | 56.3 | -4 |
| C | 51.3 | -12.6 |
| D | 51.0 | -13.3 |

| | % Fake Tracks | % Change |
|---|---|---|
| A | 7.7 | - |
| B | 8.9 | +16% |
| C | 9.5 | +23% |
| D | 8.7 | + 13% |

# Higgs discovery vs Btag eff.

- B tagging is critical for light Higgs discovery
- Higgs working group found direct relationship (significance∝L*eff$^2$).
- For a 4% reduction in b-tag efficiency (CDF and D0)
    - ~ 3 GeV less mass reach
    - ~ 8% more luminosity is required



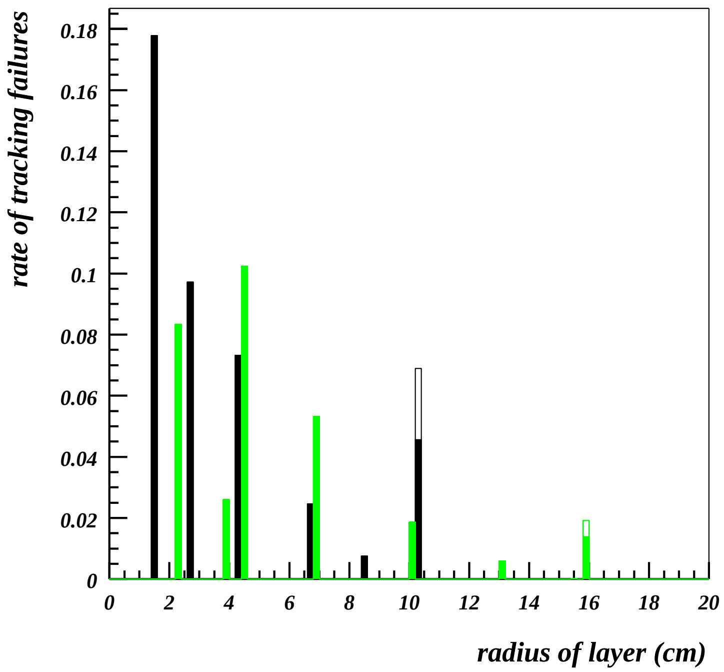

Relative b-tag efficiency (1= 65%)

# Effect of dropping layer 4 or 5

- Reduction in b tag eff. from dropping an outer layer could be compounded by degraded COT performance due to aging and/or high occupancies
- The quoted 4% reduction represents a minimum!
    - additional fakes (16%) would force tighter cuts and reduced efficiencies
    - Multiple interactions at high luminosity will become problematic
    - The effect will be greater for stand alone tracking (which is used for the forward region or ~30% of acceptance)
- Dropping layer 4 or 5 layer would require more luminosity, or would lower the discovery mass reach by >~3 GeV

# Comparison to Run IIa

- Tracking failures in R-phi view

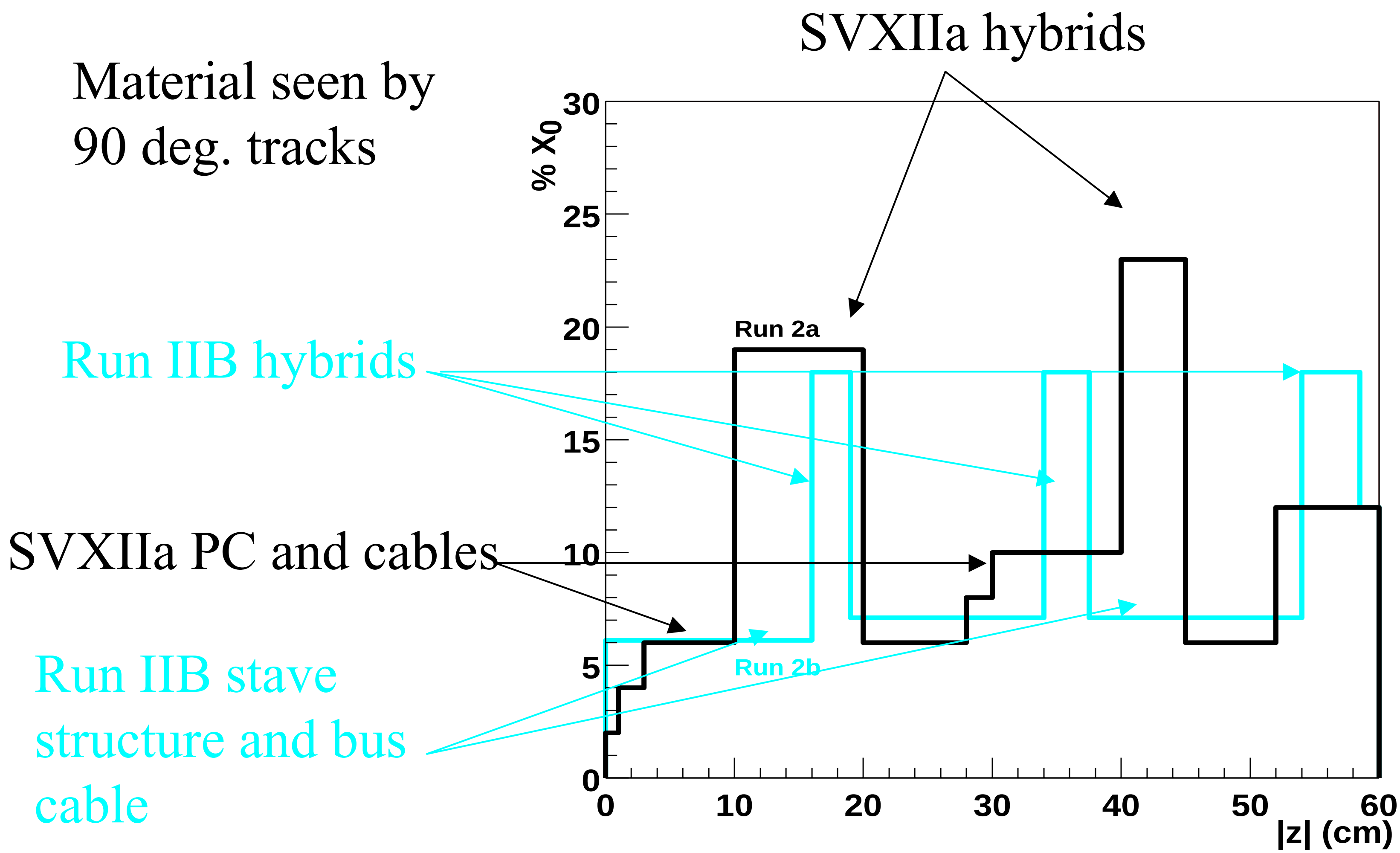


# Stave Material and Stiffness

- Stiffness traded for light construction
- Average materials over area of stave: 1.8% X0 per stave:
  - 42% of total is in silicon sensors (2 sensors 320um thick =0.64X0)
  - 33% in CF, cooling tubes, water, glue
  - 12% in hybrids
  - 9% in bus cable
  - 4% in MiniPC (actually outside tracking region)
- Can tolerate ±80μm radial deviation from a plane over a module (~20cm )
- FEA of structure found that sag was ~170μm over 60 cm length
- Making prototypes to verify FEA results – reasonable agreement

# Compare Material in Run IIA with IIB

Material seen by 90 deg. tracks

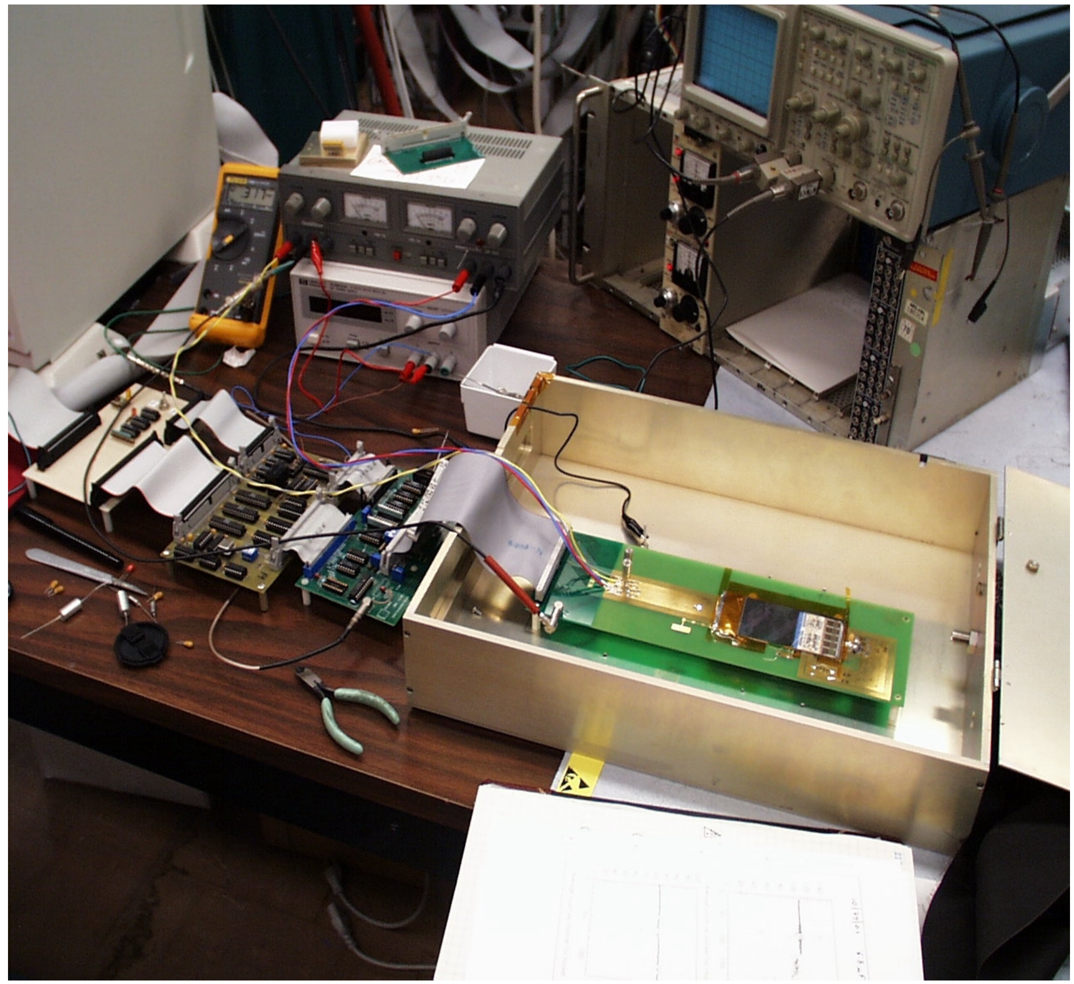


# Electrical Prototyping of Stave Bus

- Proposed stave concept uses a data, control, and power distribution bus which is placed underneath the silicon detectors.
  - Potential capacitive coupling of digital signals into the detector backplane and SVX4 front ends.
- Issue is particularly for deadtimeless operation
- Basic approach to control of coupling:
  - Shielding and insulation layer thickness
  - grounding and power distribution
  - pulse shapes, timing, and current
  - Challenge is to minimize coupling while maintaining low mass bus.
  - Bus prototype has been constructed and study is under-way

# Electrical Bus Prototype tests

- Pre-prototype bus built into G10 board
- Use leftover SVX' layer 4 sensor (single sided) and SVXII hybrid
- Test setup at LBL used to study different configurations of grounding and shielding



# Prototype Stave Bus Findings:

- Without shield

  clear coupling can be seen and spatially correlated with specific activity on bus (clocks, data buses, etc)
- With 10 micron Al foil (assumed in material estimates)

  all spatial effects are erased. Some overall coupling remains.
- Pedestal shifts seen during mode transitions when power consumption changes can be reduced by grounding changes and bypassing.
- Further improvement expected from changes in grounding and signal conditioning. Present shield thickness is probably sufficient.

# Electrical Bus Prototype tests

- Pre-prototype bus built into G10 board
- Use leftover SVX' layer 4 sensor (single sided) and SVXII hybrid
- Test setup at LBL used to study different configurations of grounding and shielding